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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/275,527	03/24/1999	DAVID KARCHMER	ALTRP049/A44	9876

22434 7590 06/05/2003

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/275,527	Applicant(s) KARCHMER ET AL.	
	Examiner Dwin M Craig	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 1999* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4 and 6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

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DETAILED ACTION

1. Claims 1-28 have been presented for reconsideration in view of Applicants Amended claim language. Claims 1-28 have been examined and rejected.

Response to Arguments

2. Applicant's arguments filed on 28 August 2003 have been fully considered. Examiners response is as follows:

2.1 Regarding Applicant's response to the granting of priority to Provisional Patent Application 60/086,153:

Applicant has argued that;

> In paragraph 4, page 2 of the Office Action mailed January 7, 2003, the Examiner stated that the "proposed drawing correction/and or the proposed substitute sheets of drawings filed on 19 May 1998 in the applicant's provisional U.S. Patent Application No. 60/086,153 have been disapproved because they introduce new matter into the drawings." The Applicant respectfully reminds the Examiner that no new matter is introduced by an original filing of a provisional application and therefore the Examiner's disapproval of the drawings based upon 37 CFR 1.121(a)(6) is unfounded.
>
> Also at page 3, fourth paragraph of the Office Action, the Examiner states that the "amendment to the specification, as compared to the priority document (provisional U.S. Patent Application No. 60/086,153 filed 24 March 19991) is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure." The Applicant again respectfully reminds the Examiner that the non-provisional application 09/275,527 was originally filed on 24 March 1999 and therefore no amendment to the specification was made. Therefore, no new matter was added by amendment as stated by the Examiner and cancellation of "new matter" as requested by the Examiner is also unfounded. Additionally, a rejection under 132 for differences between a provisional and a non-provisional is improper since the provisional, by definition, only provides priority for claims that it supports.

Examiner respectfully disagrees with Applicant's position. The Examiner does not agree with Applicant's arguments relating to priority to provisional application No. **60/086153** because Applicant's non-provisional application introduces new matter in the form of **Figures (1A, 1B, 2A, 2B, 2C, 3A, 3B, 4A, 5A, 5B, 5C, 6, 7, 8A, 8B, 9A, 9B, 10A, 10B, 11A, 11B, 12, 13, 14, 15,**

16) and corresponding text. Therefore the Claims that rely on this new matter for enablement and written description are not afforded priority to the provisional application. The Examiner asserts that the non-provisional application has 34 pages of descriptions as well as 27 figures as discussed above, the provisional application has only 3 pages of text, most of which consist of source code listings of VHDL and VERILOG as well as 2 figures of which only a version of provisional application No. **60/086153** figure 2 is incorporated as non-provisional application No. **09/275527** Figure 4B. The Examiner asserts that the non-provisional application introduces new matter, which is essential for enablement of Applicant's claims and therefore the Examiner asserts that the claims that require support from the non-provisional Application should not receive the benefit of claiming priority back to the filing date of Applicant's provisional application, as acknowledged by Applicant.

2.2 Regarding Applicant's response to the 35 U.S.C. 112 1st paragraph rejections of Claims 1-28:

Applicant has argued that;

> All claims were rejected under 35 U. S. C. 112, first paragraph, as containing subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor, at the time the application was filed, had possession of the claimed invention. The Applicant believes that the provisional application properly provides support for all claims in non-provisional application.

The Examiner respectfully disagrees with Applicant's argument that provisional application No. **60/086153** supports Applicant's claimed invention. The Examiner asserts, as an example, that no where in non-provisional application No. **60/086153** is the support disclosed for, *"a method of creating a behavioral model to allow non-atomic behavioral simulation of process blocks in an electronic design the method comprising: annotating the ADD*

representation of the process block with one or more control nodes wherein when a particular control node is encountered, a state within the process block associated with the control node can be directly observed thereby substantially eliminating an atomic nature of the process block so as to provide a non-atomic analysis of the behavioral model" where in provisional application No. **60/086153** is the distinction made between atomic and non-atomic nature of the process block disclosed? The Examiner does not see where the term *Assignment Decision Diagram* is disclosed in the Applicant's provisional application. The Examiner asserts that nowhere in Applicant's provisional application is any method, apparatus, and computer executable source code, pseudo code or flow-chart disclosed that teaches how the process block is to be observed. The Examiner asserts that nowhere in Applicant's provisional application is the support for Claims 2's language wherein the Applicant claims, *"an assignment value portion representing the computation of values that are to be assigned to a storage unit of an output port, wherein the values are computed from current contents of storage units, input ports, or constants provided to the ADD;"* Examiner needs to know where in Applicant's provisional application is support for the storage units, input ports or constants, where is the support for showing how the these values are computed. The Examiner has found Applicant's arguments to be unpersuasive and therefore uphold the earlier 35 U.S.C. 112 1st paragraph rejections of Claims 1-28 in regards to Applicant's provisional application No. **60/086153.**

2.3 Regarding Applicant's response to the Examiner's requirement to provide the reference *("Assignment Decision Diagrams for High-Level Synthesis" by Viraphol Chaiyakul and Daniel D. Gajski, Technical Report #92-102);*

The Applicant has argued that:

At page 3, second paragraph of the Office Action, the Examiner states that incorporating by reference "Assignment Decision Diagram for High-Level Synthesis" by Viraphol Chaiyakul and Daniel D. Gajski, Technical Report #92-102, December 12, 1992 was improper due to the belief of the Examiner that the cited reference was essential matter. The Applicant, however, disagrees with the Examiner since the reference is "subject matter referred to for purposes of indicating the background of the invention or illustrating the state of the art." (see MPEP 608.01(p)(A)) The reference was cited as a convenience for the reader and is therefore nonessential subject matter that can be incorporated by reference.

The Examiner asserts that the *Chaiyakul et al.* reference is essential subject matter that is required to provide enablement to Applicant's claimed subject matter. The Examiner acknowledges the IDS provided by the Applicant.

2.4 Regarding Applicant's response to Examiner Claim Interpretation:

The Applicant has argued that:

At page 4, the Examiner stated that it is his belief that the term "non-atomic refers to Hardware Description Language (HDL) source code that is used in a behavioral circuit simulation." The Applicant respectfully disagrees since the term "atomic" is an adjective that is clearly defined at page 3 second paragraph of the specification, "By atomic, it is meant that the process block can not be analyzed beyond the inputs (stimuli) provided and the corresponding outputs generated" thereby restricting the ability of the circuit designer to adequately characterize, debug, and/or analyze the complex digital circuit being simulated. Therefore, the term non-atomic does not refer to source code itself but rather is an adjective that refers to a **process block that can be analyzed** beyond the inputs and corresponding outputs generated.

The Examiner asserts that Applicant's argument is persuasive and appreciates Applicant's clarification of the term *"atomic"* in regards to Applicant's claim language.

2.5 Regarding Applicant's response to Examiner's 35 U.S.C. 103(a) rejections of Claims 1, 2 and 6;

Applicant has argued that:

Claims 1, 2, and 6 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,296,467 issued to Chang in view of "Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski (hereinafter Chaiykul) and further in view of U.S. Patent 5,920,711 issued to Seawrite et al. It should be noted that the Chang reference was filed 30 September 1999 taking priority from provisional

application 60/102,566 filed 30 September 1998. Accordingly, since the Applicant believes that the instant application properly takes priority from provisional Application No. 60/086,153 filed on 19 May 1998, the Chang reference is therefore not prior art and cannot be used to render the rejected claims unpatentable. However, even in the event that the Chang reference is prior art, the Chang reference taken with the secondary references do not render claims 1, 2, and 6 as being unpatentable for at least the following reasons.

Chang describes a block based design methodology for designing a circuit system that includes selecting a plurality of pre-designed circuit blocks. These circuit blocks are strictly atomic in nature in that the block cannot be analyzed beyond the input stimuli and the corresponding outputs generated. At no point does Chang even remotely suggest determining a state within a particular circuit block since the system of Chang only involves determining output behavior based upon provided input stimuli. For example, at column 12, lines 56 - 60, "It can be used to examine a subset of chip behaviors or block interactions which need to be studied in detail to guarantee sufficiency or to guarantee that resolution provided by any existing simulation model for the block is sufficient." In this way, **Chang only references behavior at the block level and does not comprehend a state or behavior within the block** therefore demonstrating the atomic nature of Chang. The *Chaiyakul* reference merely provides a general description of the ADD and does not teach or reasonably suggest annotating the ADDs described with control nodes that provide a window into the state of the ADD at a particular point associated with the control node. The Examiner attempts to overcome this acknowledged (by the Examiner) deficiency by citing *Seawrite* which merely provides a breakpoint and does not teach or reasonably suggest the use of a control node to provide access to or control of a state within the ADD as does the invention described in more detail below.

The invention as recited in claim 1 requires,

> "Converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used by a simulator to simulate behavior of the process block; and annotating the ADD representation of the process block with one or more control nodes wherein when a particular control node is encountered, **the state within the process block associated with the control node can be directly observed** thereby substantially eliminating an atomic nature of the process block so as to provide a non-atomic analysis of the behavioral model." (Emphasis added)

Therefore, in contrast to the cited references, the invention as recited in claim 1 describes a non-atomic "annotated assignment decision diagram" approach to logic simulation by use of control nodes annotating an associated assignment decision diagram. By annotation it is meant that selected portions of a particular ADD are associated with any of a number of control nodes which can be used to stop, start, view, etc. the state of the ADD at any selected point within the ADD. Therefore, the control nodes afford the ability to observe the states **within** a particular process block and not just the global (i.e., atomic) state of a process block as required by the cited references. By affording the ability to observe a state within a process block, the logic simulation provided by the invention is more easily

debugged and provides a more detailed description of the process being simulated than is possible by any approach contemplated by the references taken singly or in any combination.

Accordingly, the Applicant believes that claim 1 is neither anticipated or rendered obvious by any of the cited references taken singly or in any combination and is therefore allowable.

The Examiner appears to be citing the filing date of the non-provisional application of 24 March 1999 and not the filing date of the provisional application of 19 May 1998.

The Examiner asserts that Applicants arguments in regards to the *Chang et al.* reference are not persuasive in that U.S. Patent **6,269,467** does qualify as prior art for the same reasons described in paragraph **2.1** above. The Examiner asserts that the atomic/non-atomic limitation that Applicant is claiming and that the Examiner is using the *Chang et al.* reference to reject under 35 U.S.C. 103 is not disclosed, enabled or otherwise supported by Applicant's provisional Application No. **60/086153** and therefore the *Chang et al.* reference is prior art in regards to this limitation. As regards the limitations of the Assignment Decision Diagrams or ADD's the Examiner relies on the *Chaiykul et al.* reference which predates Applicants provisional application filing date.

Applicant persuasively asserts that the *Chang et al.* reference does not disclose process blocks that cannot be analyzed beyond the input stimuli and the corresponding outputs generated. The Examiner withdraws the earlier 35 U.S.C. 103 rejection of Claims 1, 2 and 6 because they depend upon the *Chang et al.* reference to reject the limitation concerning the non-atomic nature of each process block.

As regards Applicant's arguments that the *Chaiyakul* reference is only a general description of ADD's the Examiner asserts that the *Chaiyakul* reference describes methods to implement the ADD's and reduce to practice this method of modeling digital logic. The

Examiner asserts that on pages 27, 28, 30-41 the *Chaiyakul* discloses scheduling and interactive usage of the ADD which implies the need for control nodes to control the scheduling and user interaction with a simulation using Assignment Decision Diagrams. The Examiner refers to the *Seawrite* reference to explicitly disclose that providing a mechanism to control the flow of a simulation is known in the art. The Examiner asserts that control nodes in process blocks are known in the art as disclosed in the *Seawrite* reference. The Applicant's arguments, as regards the *Chaiyakul* and *Seawrite* references, are unpersuasive and the Examiner upholds the rejections of the specific limitations in regards to these references.

2.6 Regarding Applicant's response to the 35 U.S.C. 103 rejections of independent Claim 7.

The Applicant has argued that:

> Independent claim 7 has been amended to recite substantially the same limitations of claim 1 albeit as a behavioral model, provided on a machine readable medium and is therefore allowable for at least the reasons stated for independent claim 1.
>
> The Examiner rejected a number of dependent claims under the above cited references further in view of U.S. Patent 6.421,808 issued to McGeer which adds nothing to the already cited references that renders any of the rejected dependent claims as unpatentable.

Applicant persuasively asserts that the *Chang et al.* reference does not disclose process blocks that cannot be analyzed beyond the input stimuli and the corresponding outputs generated. The Examiner withdraws the earlier 35 U.S.C. 103 rejection of Claim 7 because the rejection depends upon the *Chang et al.* reference to reject the limitation concerning the non-atomic nature of each process block. The Examiner assets that the *McGeer* reference does provide teaching of the use of control nodes and find Applicant's arguments in regards to the *McGeer, Chaiykul* and the *Seawrite* references to be unpersuasive.

2.7 Regarding Applicant's response to the 35 U.S.C. 103 rejection of Claims 11-26:

Applicant has argued that:

> The Examiner rejected claims 11 - 26 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,937,190 issued to Gregory (hereinafter referred to as Gregory 1) in view of U.S. Patent 5,870,608 issued to Gregory further in view of Chaiykul and further in view of McGeer. Gregory 1 teaches architecture and methods for hardware description language source level analysis and does not teach or even remotely suggest use of control nodes to provide a non atomic view of a state within a particular process block.
>
> Independent claim 11 recites in part,
>
> "(f) annotating the assignment decision diagram (ADD) with a plurality of selected control nodes that are responsible for maintaining control flow through the simulator, wherein when a particular control node is encountered, a state within the process block associated with the control node can be directly observed thereby substantially eliminating an atomic nature of the process block"
>
> Therefore, in contrast to the cited references, the invention as recited in claim 11 describes a non-atomic "annotated assignment decision diagram" approach to logic simulation by use of control nodes annotating an associated assignment decision diagram. Therefore, the control nodes afford the ability to observe the states **within** a particular process block and not just the global (i.e., atomic) state of a process block as required by the cited references. Since none of the secondary references teach or even remotely suggest control nodes to view an internal state of a process block, the Applicant believes that claim 11 and its associated dependent claims 12 - 26 are allowable over the cited references taken singly or in any combination.

The Examiner asserts that as stated in section **2.5** that the *Chaiykul* reference implies the use of Control nodes and that the use of control nodes to control the flow of a simulation is known in the art. The Examiner respectfully directs Applicant's attention to **Figures 11 and 12 of U.S. Patent 5,937,190 Gregory et al.** where there is disclosed a sample of source code followed by a decision tree of CONTROL nodes **(Figure 12).** The Examiner finds Applicant's arguments in regards to **Gregory et al. U.S. Patent 5,937,190** not teaching CONTROL nodes to be unpersuasive. The Examiner respectfully directs Applicant's attention to **Figure 60** of **U.S. Patent 5,937,190** where a non-atomic mapping is disclosed of Control nodes, HDL source code,

and the simulation. The Examiner respectfully directs Applicant's attention to **Figure 52** of **U.S. Patent 5,937,190** where the ability to go between non-atomic and atomic levels of a simulation is provided via the *Logic Levels* and *ZOOM IN*, and *ZOOM OUT* buttons on the Logic Inspector User Interface Window. The Examiner respectfully directs Applicant to **Figure 58** of **U.S. Patent 5,937,190** where the diagram shows a Parse Tree of CONTROL nodes. The Examiner has found Applicant's arguments in regards to the 35 U.S.C. 103 rejection of Claims 11-26 to be unpersuasive and therefore upholds the earlier rejection.

2.8 Regarding Applicant's response to the 35 U.S.C. 103 rejection of Claims 27 and 28:

The Applicant asserts that:

> The Examiner rejected claims 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,848,236 issued to Dearth in view of U.S. Patent 5,937,190 issued to Gregory further in view of Chaiykul. Dearth simply teaches computer program product that specifies a method of compiling a simulation object used by a simulator to simulate the operation of a digital circuit and does not teach or even remotely suggest use of control nodes to provide a non-atomic view of a state within a particular process block. Since none of the secondary references teach or even remotely suggest control nodes to view an internal state of a process block, the Applicant believes that claims 27 and 28 are allowable over the cited references taken singly or in any combination.

The Examiner asserts that the *Chaiykul* reference implies the use of control nodes for scheduling, *(see response to arguments section2.5)*. As regards Applicant's statement that the *Dearth* reference, *"simply teaches < a> computer program product"* the Examiner asserts that a computer programming product is what Applicant is claiming in independent Claim **27**. The Examiner asserts that the **Gregory U.S. Patent 5,937,190** discloses atomic and non-atomic views of a simulated circuit *(see the response to arguments section 2.7 above)*. The Examiner asserts that the **Dearth U.S. Patent 5,848,236** reference does not expressly disclose a non-

atomic view of a process block as recited by Applicants amended Claim language. Applicant persuasively asserts that the *Dearth* reference does not disclose process non-atomic view of process blocks and therefore withdraws the earlier 35 U.S.C. 103 rejections of Claims **27** and **28.**

Drawings

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 19 May 1998 in applicant's provisional U.S. Patent Application No. **60/086,153** have been disapproved because they introduce new matter into the drawings. 37 CFR 1.121(a)(6) states that no amendment may introduce new matter into the disclosure of an application. The original disclosure does not support the showing of the elements that are disclosed in Applicant's drawings submitted on 24 March 1999.

Specification

4. The attempt to incorporate subject matter into this application by reference *("Assignment Decision Diagrams for High-Level Synthesis" by Viraphol Chaiyakul and Daniel D. Gajski, Technical Report #92-102, December 12, 1992 see page 15, Lines 14-17 of Applicants Specification)* is improper because;

> The incorporation of essential material in the specification by reference to a foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicant, or a practitioner representing the applicant, stating that the amendatory material consists of the same material incorporated by reference in the referencing application. See *In re Hawkins*, 486 F.2d 569, 179 USPQ 157 (CCPA 1973); *In re Hawkins*, 486 F.2d 579, 179 USPQ 163 (CCPA 1973); and *In re Hawkins*, 486 F.2d 577, 179 USPQ 167 (CCPA 1973).

...as per the MPEP paragraph 6.19.

5. The specification, as compared to the priority document (provisional U.S. Patent Application No. **60/086,153** filed on 24 March 1999), is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure that is not disclosed in the priority document. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure, the priority document, is as follows: **Figures 1-16, Specification (pages 1-34) and the Claims submitted on 24 March 1999 in the Non-Provisional Application number 09/275527.**

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. **Claims 1-28** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. All of the figures and written descriptions were not disclosed in Applicant's original provisional U.S. Patent Application No. **60/086,153** filed on 19 May 1998, and therefore the non-provisional application is new matter and as such is non-enabling for **Claims 1-28**.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 1, 7, 11, 27 and 28** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term *"substantially* is ambiguous.

Furthermore, the term "*substantially*" in **Claims 1, 7, 11, 27 and 28** is a relative term which renders the claims indefinite. The term "*substantially*" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. It is unclear to the Examiner to what level of abstraction a substantially eliminated atomic nature of a process block will be.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1, 2 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rostoker et al. U.S. Patent 5,623,418** in view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference, and in further view of **Seawrite et al. U.S. Patent 5,920,711.**

8.1 As regards **Claims 1** the *Rostoker et al.* reference discloses a behavioral model **(Figure 2 Item 6, Figure 12 Item 1212, Col. 2 Lines 35-49, Col. 7 Lines 18-25)** and non-atomic behavioral simulation of process blocks in an electronic design **(Figures 25a, 25b, 30a, 30b, 30c, 30d, 31, Col. 4 Lines 13-42, Col. 6 Lines 33-38, Col. 15 Lines 35-61, Col. 16 Lines 8-16),** receiving hardware design code describing a process block **(Col. 16 Lines 38-64)** and interactive design with access to any node in the design **(Col. 6 Lines 25-32).**

The *Rostoker et al.* reference does not expressly disclose, converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, thereby creating one or more break points that allow the simulator to stop at associated points in the process block.

The *Chaiykul et al.* reference discloses converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, **(Pages 10-24).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have combined the *Rostoker et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

The *Rostoker et al.* reference does not expressly disclose creating one or more break points that allow the simulator to stop at associated points in the process block.

The *Seawright et al.* reference teaches, creating one or more break points that allow the simulator to stop at associated points in the process block **(Figure 44, Items 4460 and 4470, and Figure 45b).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *Seawright et al.* reference because a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

8.2 As regards **Claim 2** the *Rostoker et al.* reference does not expressly disclose assignment decision diagrams.

The *Chaiykul et al.* reference discloses assignment decision diagrams **(Pages 1-49).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

As regards **Claim 6** the *Rostoker et al.* reference does not expressly disclose, VHDL or Verilog.

The *Seawright et al.* reference teaches VHDL or Verilog **(Figure 59, Item 2706).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *Seawright et al.* reference because *(motivation to combine)* a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

9. **Claims 3, 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rostoker et al. U.S. Patent 5,623,418** in view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference, and in further view of **Seawrite et al. U.S. Patent 5,920,711** and in further view of **McGeer et al. U.S. Patent 6,421,808.**

9.1 As regards all of independent **Claim 1's** limitations, were addressed in paragraph **8.1** above.

9.2 As regards **Claim 3** the Examiner asserts that the *Rostoker et al.* reference does disclose control nodes and process trees **(Rostoker et al. U.S. Patent 5,623,418 Figure 10 ITEM 1006, Figure 11, Figures 13-15)**, *see the rejection in paragraph 8.1 above*;

However, the *Rostoker et al.* reference does not expressly disclose;

A control node being selected from a group of control nodes,

The selected control node representing a conditional branch in the control flow of the simulation,

A null control node used as a place holder,

A suspend node used to suspend execution of a process block.

The *McGeer et al.* reference discloses control nodes and groups of control nodes, the selected control node representing a conditional branch in the control flow of the simulation, a null control node used as a place holder, a suspend node used to suspend execution of a process block **(Figure 11, 14-17, 28 and Col. 2 Lines 56-57, Col. 36 Lines 17-20, Figure 11-24, Col. 22 Lines 52-67, Col. 23 Lines 25-50, Col. 33-41).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

9.3 As regards **Claim 4** the *Rostoker et al.* reference does not expressly disclose;

The suspend control node is selected from a group comprising an event type suspend control node used to suspend execution of the process block pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specified length of time.

The *McGeer et al.* reference discloses, the suspend control node is selected from a group comprising an event type suspend control node used to suspend execution of the process block, **(Figure 11, 14-17, 28 and Col. 2 Lines 56-57, Col. 36 Lines 17-20, Figure 11-24, Col. 22 Lines 52-67, Col. 23 Lines 25-50, Col. 33-41).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The *Rostoker et al.* reference does not expressly disclose pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specified length of time.

The *Seawrite et al.* reference discloses, pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specified length of time **(Figure 16, 23, 24, 25, 26, 34, 44, 45a, 45b, 45c).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *Seawright et al.* reference *(motivation to combine)* because a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

9.4 As regards **Claim 5** the *Rostoker et al.* reference does not expressly disclose;

Synthesizing a circuit level parse tree upon operational characteristics and schematic layout of the circuit being simulated contained within the hardware design code, wherein the parse tree includes a process token and a process block token, the process token identifying a simulation process to be carried out within the process block;

Traversing the parse tree and allocating a process block structure in the simulation object file when the process block token is encountered.

Further traversing the parse tree to determine if the process token is available.

Determining the type of simulation process identified by the process token.

Converting the identified simulation process to a corresponding ADD.

Annotating the ADD with a plurality of selected control nodes that are responsible for control flow through the simulator wherein each of the control nodes has a pointer and the control nodes are stored in a list.

The *McGeer et al.* reference discloses; Synthesizing a circuit level parse tree upon operational characteristics and schematic layout of the circuit being simulated contained within

the hardware design code, wherein the parse tree includes a process token and a process block token, the process token identifying a simulation process to be carried out within the process block;

Traversing the parse tree and allocating a process block structure in the simulation object file when the process block token is encountered.

Further traversing the parse tree to determine if the process token is available.

Determining the type of simulation process identified by the process token.

(Figures 14-29, Col. 30 Lines 20-67, All of Columns 31-50, Col. 51 Lines 1-63).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The *Rostoker et al.* reference does not expressly disclose, Converting the identified simulation process to a corresponding ADD, annotating the ADD with a plurality of selected control nodes that are responsible for control flow through the simulator wherein each of the control nodes has a pointer and the control nodes are stored in a list.

The *Chaiykul et al.* reference discloses Converting the identified simulation process to a corresponding ADD, annotating the ADD with a plurality of selected control nodes that are responsible for control flow through the simulator wherein each of the control nodes has a pointer and the control nodes are stored in a list **(Pages 1-49).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

10. **Claims 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rostoker et al. U.S. Patent 5,623,418** in view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference, and in further view of **Seawrite et al. U.S. Patent 5,920,711.**

10.1 As regards **Claims 7 and 8** the the *Rostoker et al.* reference discloses a behavioral model **(Figure 2 Item 6, Figure 12 Item 1212, Col. 2 Lines 35-49, Col. 7 Lines 18-25)** and non-atomic behavioral simulation of process blocks in an electronic design **(Figures 25a, 25b, 30a, 30b, 30c, 30d, 31, Col. 4 Lines 13-42, Col. 6 Lines 33-38, Col. 15 Lines 35-61, Col. 16 Lines 8-16),** receiving hardware design code describing a process block **(Col. 16 Lines 38-64)** and interactive design with access to any node in the design **(Col. 6 Lines 25-32)** and machine readable medium **(Figures 16, 17, 24, 29 Item 2914, Col. 2 Lines 66-67, Col. 3 Lines 1-20).**

10.2 As regards **Claim 7,** the *Rostoker et al.* reference does not expressly disclose, converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, thereby creating one or more break points that allow the simulator to stop at associated points in the process block.

The *Chaiykul et al.* reference discloses converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, **(Pages 10-24).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

10.3 As regards **Claim 8** the *Rostoker et al.* reference does not expressly disclose, creating one or more break points that allow the simulator to stop at associated points in the process block.

The *Seawright et al.* reference teaches, creating one or more break points that allow the simulator to stop at associated points in the process block **(Figure 44, Items 4460 and 4470, and Figure 45b).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *Seawright et al.* reference because a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

11. **Claims 9 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rostoker et al. U.S. Patent 5,623,418** in view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the

Chaiykul et al. reference, and in further view of **Seawrite et al. U.S. Patent 5,920,711** and in further view of **McGeer et al. U.S. Patent 6,421,808.**

11.1 As regards all of independent **Claim 7's** limitations, were addressed in paragraph **10.1** above.

11.2 As regards **Claim 9** the *Rostoker et al.* reference does not expressly disclose; the control node being selected from a group of query control nodes used to represent conditional branches in control flow, an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder, and a suspend control node used to suspend execution of the process block.

The *McGeer et al.* reference discloses; the control node being selected from a group of query control nodes used to represent conditional branches in control flow, an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder, and a suspend control node used to suspend execution of the process block **(Figure 11, 14-17, 28 and Col. 2 Lines 56-57, Col. 36 Lines 17-20, Figure 11-24, Col. 22 Lines 52-67, Col. 23 Lines 25-50, Col. 33-41).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

11.3 As regards **Claim 10** the *Rostoker et al.* reference does not expressly disclose; the suspend control node is selected from the group comprising an event type suspend control

node used to suspend execution of the process block pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specific length of time, although the *Rostoker et al.* reference does disclose control nodes *(see rejection in paragraph 8.1 above)*.

The *Seawrite et al.* reference discloses, an event type suspend control node used to suspend execution of the process block pending a pre-determined future event and a delay type suspend control node used to suspend execution of the process block for a specific length of time **(Figure 16, 23, 24, 25, 26, 34, 44, 45a, 45b, 45c).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Rostoker et al.* reference with the *Seawright et al.* reference because *(motivation to combine)* a designer would like to be able to debug the design at the protocol level of abstraction ***(Seawrite et al. Col. 2 Lines 47-50).***

12. **Claims 11-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gregory et al. U.S. Patent 5,937,190** *hereafter referred to as G1* in view of **Gregory U.S. Patent 5,870,608** *hereafter referred to as G2* and in further view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference and in further view of **McGeer et al. U.S. Patent 6,421,808.**

12.1 As regards **Claim 11** the *G1* reference discloses a method of compiling a simulation object file to simulate the operation of a digital circuit **(Figure 1, 3 Item 154, Col. 6 Lines 37-64),** wherein the simulation object file represents a behavioral model process block

arranged to simulate the operation of the digital circuit by providing an output signal based on the input signal **(Figures 4-8, 43-44, Col. 3 Lines 9-21)** comprising;

(a) A parse tree, which includes a token, and a token based hierarchy, wherein the token identifies a process block wherein there is code describing the circuit being simulated, **(Figures 2-12, Figure 58 Item 6004, specifically, Figure 5-bottom of figure, Col. 11 Lines 4-15).**

(b) Traversing the parse tree and allocating a process block structure in the simulation object file when a token is encountered **(Figures 5-9, 35, 36, 39, 60 and Col. 8 Lines 60-68, Col. 9 Lines 1-46, Col. 17 Lines 11-31, Col. 21 Lines 1-4, Col. 21 Lines 35-56, Col. 25 Lines 45-58),**

(d) Determining the type of simulation process identified by the token **(Col. 18 Lines 49-62, Col. 3 Lines 22-37).**

The *G1* reference discloses a non-atomic view of a process block **(Figure 52)**.

The *G1* reference does not expressly disclose,

(c) Further traversing the parse tree to find an available token.

(e) Converting the simulation process to an assignment decision diagram.

(f) Annotating the assignment decision diagram with a plurality of selected control nodes which control the flow through the simulation, wherein said control nodes have a pointer to the next control node that is used to proceed through to the next step in the simulation process wherein the control nodes are stored in a process block control node list contained in the object file.

The *G2* reference discloses;

(c) Further traversing the parse tree to find an available token **(Figure 4 Item 1009).**

...a plurality of selected control nodes which control the flow through the program, wherein said control nodes have a pointer to the next control node that is used to proceed through to the next step in the process wherein the control nodes are stored in a process block control node list contained in the object file **(Figures 1, 4-6, and Col. 3 Lines 26-67, Col. 4 Lines 1-44, Col. 10 Lines 50-67,Col. 51, 52, 69, 70, 71, 72, 85, 86, 87, 88, 95, 96, 117, 118, 125, 126, 129, 130,149, 150, 151, 152, 159, 160, 197, 198, 245, 246, 247, 248, 249, 250, 293, 294, all of 372, 373 and 374).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the ***G2*** reference because, the ***G1*** reference refers to the ***G2*** reference in its specification ***(G2, Col. 8 Lines 28-38).***

The ***G1*** reference does not expressly disclose, converting the simulation process to an assignment decision diagram.

The *Chaiykul et al.* reference discloses Converting the simulation process to an assignment decision diagram **(Pages 10-24).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the ***G1.*** reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

The ***G1*** reference discloses sub-parse trees **(Figure 9, Items 39101, 39103, 39102, 39104, 39105 and 39106).**

12.2 As regards **Claim 13** the ***G1.*** reference does not expressly disclose, an assignment decision diagram, an assignment value portion assigned to an output port, as assignment condition connected to a data flow path such that the end condition is either TRUE or FALSE, an assignment decision node.

The *Chaiykul et al.* reference discloses an assignment decision diagram, an assignment value portion assigned to an output port, as assignment condition connected to a data flow path such that the end condition is either TRUE or FALSE, an assignment decision node **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

12.3 As regards **Claim 14,** the ***G1*** reference does not expressly disclose, a control node selected from a group of query control node used to represent a conditional branch in a control flow, an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder and a suspend control node used to suspend execution of a process block.

The *McGeer et al.* reference discloses, a control node selected from a group of query control node used to represent a conditional branch in a control flow **(Figure 11, 14-17, 28 and Col. 2 Lines 56-57, Col. 36 Lines 17-20),** an evaluation/assignment control node used to represent an assignment operation, a null control node used as a place holder and a suspend

control node used to suspend execution of a process block, **(Figure 11-24, Col. 22 Lines 52-67, Col. 23 Lines 25-50, Col. 33-41).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *G1* reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

12.4 As regards **Claims 15 and 16** the *G1* reference discloses a suspend node with an event type suspend control node used to suspend execution of the process block pending a pre-determined future event and wherein the suspend node comprises; a delay type suspend control node to suspend execution of the process block for a specific length of time. **(Col. 21 Lines 18-67, Col. 22 Lines 1-67).**

12.5 As regards to **Claim 17,** the *G1* reference does not expressly disclose, pointers and tokens.

The *Gregory* reference discloses pointers and tokens **(Figures 1, 4-6, and Col. 3 Lines 26-67, Col. 4 Lines 1-44, Col. 10 Lines 50-67,Col. 51, 52, 69, 70, 71, 72, 85, 86, 87, 88, 95, 96, 117, 118, 125, 126, 129, 130,149, 150, 151, 152, 159, 160, 197, 198, 245, 246, 247, 248, 249, 250, 293, 294, all of 372, 373 and 374).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *G1* reference with the *G2* reference because, the *G2* reference refers to the *G1* reference in its specification ***(Gregory, Col. 8 Lines 28-38).***

12.6 As regards **Claim 18** the ***G1*** reference does not expressly disclose, converting a true sub-parse tree to a true conditional ADD and converting false sub-parse tree to a corresponding false conditional ADD.

The *Chaiykul et al.* reference discloses converting a true sub-parse tree to a true conditional ADD and converting false sub-parse tree to a corresponding false conditional ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

12.7 As regards **Claim 19** the ***G1*** reference does not expressly disclose mapping the control nodes.

The ***G2*** reference discloses mapping the control nodes **(Col. 372 Lines 48-67 and Col. 373 Lines 1-2).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the ***G2*** reference because, the ***G2*** reference refers to the ***G1*** reference in its specification ***(Gregory, Col. 8 Lines 28-38).***

As regards **Claim 20** the ***G1*** reference does not expressly disclose, a process loop type token, the loop process having a loop entry condition and a loop exit condition suitable for entering and exiting a corresponding loop expression and loop body, allocating a query control node to the process control node list.

The *McGeer et al.* reference discloses a process loop type token, the loop process having a loop entry condition and a loop exit condition suitable for entering and exiting a corresponding loop expression and loop body, allocating a query control node to the process control node list **(Figure 22, Col. 25 Lines 6-67, Col. 26 Lines 1-36, Col. 37 Lines 40-51, Col. 39 Lines 48-67, Col. 40 Lines 1-67, Col. 41 Lines 1-5).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The ***G1*** reference does not expressly disclose, converting loop expression sub-parse tree to a corresponding loop expression ADD and recursively converting the loop body sub-parse tree to a loop body ADD.

The *Chaiykul et al.* reference discloses converting loop expression sub-parse tree to a corresponding loop expression ADD and recursively converting the loop body sub-parse tree to a loop body ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

12.8 As regards **Claim 21** the ***G1*** reference does not expressly disclose, pointers, control nodes and mapping.

The *McGeer et al. reference* discloses pointers, control nodes and mapping **(Figures 14, 15 and 35, Col. 5 Lines 40-54).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The ***G1*** reference does not expressly disclose, mapping the control node to an ADD.

The *Chaiykul et al.* reference discloses mapping the control node to an ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

12.9 As regards **Claims 22 and 23** the ***G1*** reference does not expressly disclose, a suspend token.

The *McGeer et al.* reference discloses a suspend token **(Col. 21 Lines 43-67).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *McGeer et al.* reference because, V++ introduces little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly ***(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).***

The ***G1*** reference does not expressly disclose, converting the control node to an ADD.

The *Chaiykul et al.* reference discloses converting the control node to an ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

12.10 As regards **Claims 24 and 25** the ***G1*** reference does not expressly disclose, converting the control node to an ADD.

The *Chaiykul et al.* reference discloses converting the control node to an ADD **(Pages 1-49).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

The ***G1*** reference does not expressly disclose, pointers, control nodes and mapping.

The *McGeer et al. reference* discloses pointers, control nodes and mapping **(Figures 14, 15 and 35, Col. 5 Lines 40-54),** allocating a query control node to the process control node list **(Figure 22, Col. 25 Lines 6-67, Col. 26 Lines 1-36, Col. 37 Lines 40-51, Col. 39 Lines 48-67, Col. 40 Lines 1-67, Col. 41 Lines 1-5).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the ***G1*** reference with the *McGeer et al.* reference because, V++ introduces

little resource overhead. In addition the shorter design cycle and smaller resource sizes can benefit large designs, improve maintainability, and provide correct designs more quickly **(McGeer et al. Col. 51 Lines 65-67 and Col. 52 Lines 1-3).**

12.11 As regards **Claim 26** the ***G1*** reference discloses a Field Programmable Gate Array **(Col. 1 Lines 33-51).**

13. **Claims 27 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dearth et al. U.S. Patent 5,848,236** in view of **Gregory et al. U.S. Patent 5,937,190** *hereafter referred to as the G1* reference and in further view of **"Assignment Decision Diagram for High Level Synthesis" by Viraphol Chaiykul and Daniel D. Gajski** here after referred to as the *Chaiykul et al.* reference.

13.1 As regards **Claim 27** the *Dearth et al.* reference discloses, A computer program project **(Col. 1 Lines 45-63)** comprising computer program instructions **(Col. 3 Lines 15-46, Col. 6 Lines 52-65)** provided on a computer readable medium **(Col. 5 Lines 43-61)**, specifying a method of compiling a simulation object **(Col. 6 Lines 66-67 and Col. 7 Lines 1-67)** used by a simulator to simulate the operation of a digital circuit **(Col. 1 Lines 35-42).**

The *Dearth et al.* reference does not expressly disclose, a behavioral model process block, synthesizing a circuit level parse tree with a process token, traversing the parse tree and allocating a process block when the token is encountered, determining the type of simulation from the token, converting the identified simulation process to a corresponding assignment decision diagram, and annotating the assignment decision diagram (ADD) with control nodes

that control flow through the simulator with pointers, wherein the pointers are stored in a process block control node list contained in the object file.

The *G1* reference discloses, a behavioral model process block **(Figure 2, Col. 1 Lines 15-20)** synthesizing a circuit level parse tree with a process token **(Figure 58 Item 6004, Figure 5-bottom of figure),** traversing the parse tree and allocating a process block when the token is encountered, determining the type of simulation from the token, **(Figures 5-9, 35, 36, 39, 60 and Col. 8 Lines 60-68, Col. 9 Lines 1-46, Col. 17 Lines 11-31, Col. 21 Lines 1-4, Col. 21 Lines 35-56, Col. 25 Lines 45-58),** with control nodes that control flow through the simulator with pointers, wherein the pointers are stored in a process block control node list contained in the object file **(Col. 8 Lines 49-59).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Dearth et al.* reference with the *G1* reference because, There has been a need for a system that allows the designer to analyze a digital circuit design in terms of the source HDL. ***(Gregory et al. Col. 8 lines 33-35).***

The *Dearth et al.* reference does not expressly disclose, converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator.

The *Chaiykul et al.* reference discloses converting the hardware design code describing the process block to an assignment decision diagram (ADD) representation that is used to simulate behavior of the process block and including one or more control nodes for maintaining control flow through the simulator, **(Pages 10-24).**

It would have been obvious to on of ordinary skill in the art, at the time of the invention, to have modified the *Dearth et al.* reference with the *Chaiykul et al.* reference because, by using Assignment Decision Diagrams the designer has the ability for estimating layout quality metrics during synthesis tasks such as allocation and scheduling ***(Chaiykul et al. Page 25).***

13.2 As regards **Claim 28** the *Dearth et al.* reference discloses an apparatus **(Figures 1, 2 and 19C, Col. 1 Lines 35-42)** and an editor **(Col. 6 Lines 43-53).**

Conclusion

14. An updated search has revealed new art. **Claims 1-28** have been rejected based on Applicant's amended claims. Independent **Claims 1, 7, 11, 27 and 28** have been rejected under 35 U.S.C. 112 2nd paragraph for being indefinite. The Examiner upholds the earlier rejections based on 35 U.S.C. 112 1st paragraph in that the *Chaiykul et al.* reference is essential for enabling Applicant's claims and that it needs to be incorporated into Applicant's specification. The Examiner upholds the rejections based on the introduction of new matter, the Examiner does not agree with Applicant that the provisional application is enabling for Applicant's claimed limitations.

14.1 Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
December 10, 2003

Copy from Examiner
Original was missing.
Dwin Craig
12-10-2003